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ABSTRACT

The possibility to develop neuromorphic computing devices able to mimic the extraordinary data processing capabilities of biological systems spurs the research on memristive systems. Memristors with additional functionalities such as robust memcapacitance can outperform standard devices in key aspects such as power consumption or miniaturization possibilities. In this work, we demonstrate a large memcapacitive response of a perovskite memristive interface, using the topotactic redox ability of La_{0.5}Sr_{0.5}Mn_{0.5}Co_{0.5}O_{3-δ} (LSMCO, $0 \leq \delta \leq 0.62$). We demonstrate that the multi-mem behavior originates at the switchable n-p diode formed at the Nb:SrTiO₃/LSMCO interface. We found for our Nb:SrTiO₃/LSMCO/Pt devices a memcapacitive effect $C_{HIGH}/C_{LOW} \sim 100$ at 150 kHz. The proof-of-concept interface reported here opens a promising venue to use topotactic redox materials for disruptive nanoelectronics, with straightforward applications in neuromorphic computing technology.

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Neuromorphic computing devices aim at mimicking biological systems and are expected to dramatically improve the performance and efficiency of electronic devices for advanced information technology.¹ Brain synapses can be emulated by memristors,^{2,3} consisting of capacitor-like structures displaying a reversible and non-volatile electrical resistance change upon the application of electrical stimulus.^{4,5} Other potential applications of memristors include nanoelectronic memories² and logic gates.⁶ Memristive behavior is ubiquitously found in transition metal oxides, including perovskite manganites.⁷ The proposed memristive mechanisms for metal/manganite systems include

the modulation of metal/insulator Schottky barriers due to oxygen vacancy (OV) electromigration,⁸⁻¹⁰ or the interfacial redox reaction occurring when a reactive electrode (Ti or Al) is used.¹¹⁻¹³ In these cases, oxygen exchange with the environment is neglected.⁹ Alternatively, reports on memristive perovskites claiming for oxygen exchange between the perovskite and the atmosphere¹⁴ or the metallic electrode¹⁵ can be found. For volumetric redox processes triggered by electrical stimuli, a robust memristive effect is expected for perovskites displaying topotactic redox ability, i.e., the capability of reversibly storing and releasing oxygen with slight structural changes that maintain

the perovskite structure.^{16,17} Here, the memristive effect relies on the electrical switch between oxidized and reduced phases with different electrical conductivities. A better stability for redox memristive behavior is envisaged for topotactic perovskites in comparison with standard ones,^{18,19} as the structure changes—i.e., change in the perovskite space group¹⁷ in the former case allows transitions between structures presenting well defined minimum energies.

Memcapacitance—non-volatile change of a device capacitance C upon the application of electrical stress is an additional functionality of memristors that has scarcely been explored.^{20–26} The proposed mechanisms include creation/annihilation of conducting nanofilaments,^{20,21} modulation of Schottky barriers at interfaces,^{21,22} oxidation/reduction of a TiO_x active layer²³ or changes in the oxide permittivity upon OV electromigration.^{24,25} While applications for memcapacitance, including neuromorphic computing devices, have been proposed,²⁷ the interest in this phenomenon has been hampered by the small reported figures to date ($C_{\text{HIGH}}/C_{\text{LOW}} \leq 10$).^{20–26} It was shown that associated capacitive networks, suitable for efficient pattern recognition, can be built from cells able to switch their capacitance between C_{HIGH} and C_{LOW} , where the array size—linked to the device computing capability—scales with a $C_{\text{HIGH}}/C_{\text{LOW}}$ ratio.²⁸ This evidences the high technological interest of memcapacitive systems with a large response.

In this paper, we show that the interface between the topotactic redox perovskite manganite $\text{La}_{0.5}\text{Sr}_{0.5}\text{Mn}_{0.5}\text{Co}_{0.5}\text{O}_{3-\delta}$ (LSMCO, $0 \leq \delta \leq 0.62$, p-type)¹⁷ and Nb:SrTiO_3 (NSTO, n-type) behaves as a switchable n-p diode with memristive and large memcapacitive behavior. We show that the observed multi-mem behavior is related to the electrical switch between LSMCO oxidized ($\delta = 0$) and reduced ($\delta \approx 0.62$) phases.

Oxidized phase LSMCO thin films were grown by laser ablation on Nb:SrTiO_3 (0.5 wt. %, 001) substrates. The growth temperature, oxygen pressure, and laser fluence were fixed at 800 °C, 0.04 mbar, and 0.5–1 J/cm², respectively. Pristine LSMCO films were ≈ 20 nm thick and epitaxial, as shown in [supplementary material Fig. S1](#). High resolution scanning transmission electron microscopy (STEM) was performed using a FEI Titan G2 microscope with a probe corrector. Microstructured top Pt electrodes, ≈ 20 nm thick, were fabricated by FIB or optical lithography. The platinum high work function (5.6 eV) allows an Ohmic interface with p-type LSMCO.²⁹ The NSTO substrate was grounded (a drop of silver paint was used to make contact) and the electrical stimulus was applied to the top Pt electrode. For the electrical characterization, we used a Keithley 2612 source-meter, an AutoLab PGSTAT302N impedance analyzer, and a standard LCR-meter.

The virgin resistances of $37.5 \times 10^3 \mu\text{m}^2$ NSTO/LSMCO/Pt devices were ~ 1 M Ω , and the current–voltage (I–V) curve for low stimulus, shown in [supplementary material Fig. S2](#), displays a rectifying behavior linked to the formation of an n-p diode at the NSTO/LSMCO interface. A forming process is triggered when a -7 V pulse is applied, resulting in a sudden resistance drop to $\sim 50 \Omega$ ([supplementary material Fig. S2](#)). After forming, dynamic I–V curves were obtained by applying a sequence of 1 ms voltage pulses of different amplitudes ($0 \rightarrow V_{\text{MAX}} \rightarrow V_{\text{MIN}} \rightarrow 0$), with the current measured during the application of the pulse. Additionally, after each voltage pulse a small reading voltage (100 mV) was applied to determine the remnant resistance states, obtaining the hysteresis switching loops (HSLs). [Figures 1\(a\)](#) and [1\(b\)](#) display typical I–V and HSL curves,

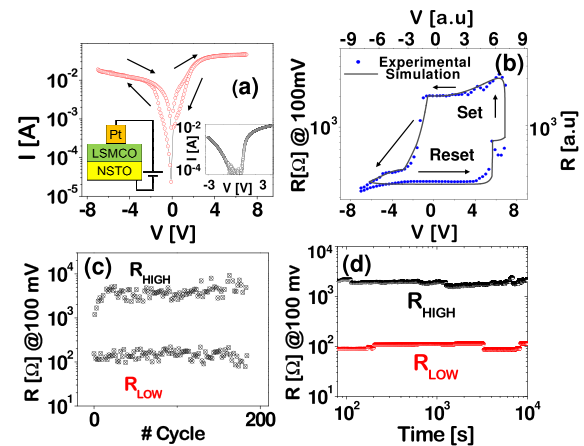


FIG. 1. (a) Dynamic pulsed I–V curve recorded on a formed device, with arrows indicating the circulation direction of the curve. The inset displays the I–V curve corresponding to a non-formed device; (b) experimental hysteresis switching loop (HSL, symbols), recorded simultaneously with the I–V curve. The simulated HSL is displayed with a solid line; (c) retention experiments corresponding to a NSTO/LSMCO/Pt device, for both R_{LOW} and R_{HIGH} states; (d) endurance test performed by applying single SET and RESET voltage pulses with opposite polarities.

both demonstrating the memristive properties of our devices. The device switches from a low resistance (R_{LOW}) to high resistive state (R_{HIGH}) (RESET process) upon the application of $\sim +5.5$ V, while the opposite behavior (SET process) is observed upon the application of ~ -1.5 V. From the second cycle, R_{HIGH} and R_{LOW} stabilize to ~ 2 –6 k Ω and ~ 100 –200 Ω , respectively, giving an average ON/OFF ratio of ~ 25 . [Figure 1\(c\)](#) shows an endurance test with a stable behavior for ~ 200 cycles, while [Fig. 1\(d\)](#) shows retention times of at least 10^4 s for both resistive states.

Interestingly, the observed memresistance is concomitant with a large memcapacitive effect. Dynamic capacitance–voltage (C–V) curves were obtained by measuring the device capacitance upon the application of DC voltage pulses of increasing amplitude with a small superimposed AC signal (10 kHz, amplitude 200 mV). [Figure 2\(a\)](#) displays dynamic C–V curves measured on devices prepared in both R_{HIGH} and R_{LOW} states. An evident difference between both curves is observed, indicating a significant capacitance change between R_{HIGH} and R_{LOW} states, where the R_{HIGH} (R_{LOW}) state corresponds to a low (high) capacitance C_{LOW} (C_{HIGH}) one. The negative capacitance found for C_{LOW} for positive voltages is attributed to the non-monotonic or positive-valued behavior of the time-derivative of the transient current in response to a small voltage step.³⁰ The memcapacitive effect was confirmed by remnant capacitance measurements, performed in both states by applying a pure AC signal at different frequencies. [Figure 2\(b\)](#) displays the evolution of both remnant C_{LOW} and C_{HIGH} states as a function of the frequency (f) of the excitation signal. $C_{\text{LOW}} \sim 3.5$ pF at 10 kHz and displays a subtle decrease with f , while C_{HIGH} displays a stronger decrease, from ~ 3 nF at 10 kHz to ~ 0.13 nF at 300 kHz. The capacitance decrease is at a higher rate for $f < 100$ kHz. The existence of leakage channels at the diode interface likely increases its effective capacitance at low f ,³¹ but other effects such as the presence of surface states might also contribute to the dependence of the capacitance with f .³² In the low frequency range, there is a rapid drop in the $C_{\text{HIGH}}/$

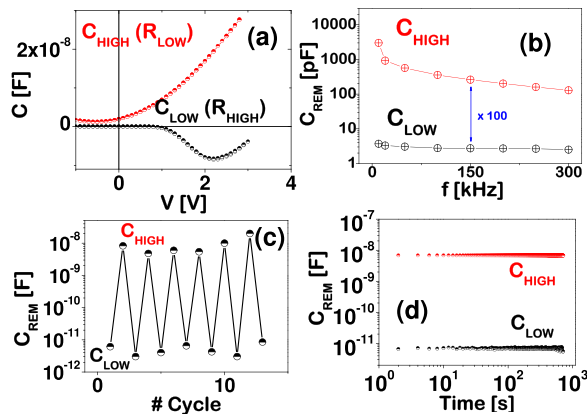


FIG. 2. (a) Dynamic capacitance–voltage (C – V) curves recorded both for oxidized (R_{LOW} and C_{HIGH}) and reduced (R_{HIGH} and C_{LOW}) LSMCO states; (b) evolution of remnant C_{HIGH} and C_{LOW} states with the frequency of the external AC signal; (c) reversible switch between C_{HIGH} and C_{LOW} (measured at 10 kHz) after the application of SET and RESET single pulses. C_{HIGH} and C_{LOW} values were in the ranges 3–20 nF and 3–9 pF, respectively; (d) retention experiments for C_{HIGH} and C_{LOW} states, measured at 10 kHz.

C_{LOW} ratio, from ~ 900 at 10 kHz to ~ 130 at ~ 100 kHz, likely due to leakage effects. For higher frequencies, leakage effects should not contribute³¹ and the dependence of C_{HIGH}/C_{LOW} with f is milder. We obtained $C_{HIGH}/C_{LOW} \sim 100$ at ~ 150 kHz, which is around one order of magnitude larger than memcapacitive figures reported to date for other systems.^{20–26} The ability of our devices to reversibly change their capacitance between two non-volatile states upon consecutive cycling is confirmed by Fig. 2(c), while Fig. 2(d) displays retention times for both C_{HIGH} and C_{LOW} higher than 10^3 s, respectively.

Figure 3(a) shows a scanning electron microscopy top-view of the device after forming, where three distinct zones are identified. Zone 1 has a diameter of $\sim 5 \mu\text{m}$ and corresponds to the contact position of the tip. Zone 2 is a ring of higher contrast than Zone 1 (diameter: $\sim 15 \mu\text{m}$) where the material from the film and the Pt electrode has been expelled during the forming process probably due to the release of O_2 gas.³³ At Zone 1, STEM-HAADF analysis shows that, upon forming, the pristine LSMCO epitaxial nanostructure [shown in supplementary material Fig. S3(a)] re-crystallizes due to selfheating effects. This re-crystallization can comprise the complete LSMCO thickness, leading to an arrangement of nanograins as the one displayed in Figs. 3(b) and S3(c). The bottom LSMCO nanograins, in contact with the NSTO substrate, retain a (001) out-of-plane orientation, while the top grains, in contact with the Pt top electrode, are in general not coherent with the bottom grains and present a tilted (001) direction, as shown in the zoomed-in image of Fig. 3(c). LSMCO re-crystallization at Zone 1 can also be partial, leading to top LSMCO non-coherent nanograins located on top of epitaxial LSMCO [see Fig. S3(c)]. The LSMCO re-crystallization process is likely driven by the presence of thermal self-accelerated effects³⁴ where both the Pt electrode [see supplementary material Figs. S3(b) and S3(c)] and (part of) LSMCO melt during electroforming, followed by a fast cooling after the end of the forming voltage that quenches melted LSMCO into a non-coherent nanograins arrangement. TEM analysis also shows that part of LSMCO becomes reduced upon during forming. Figure 4

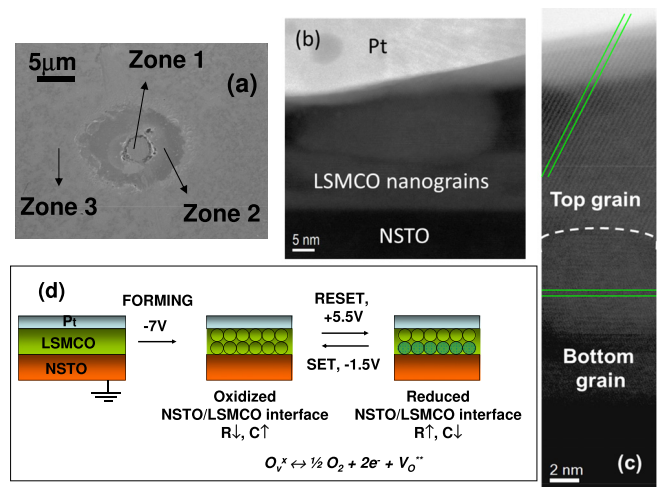


FIG. 3. (a) Scanning electron microscopy image (top-view) of a formed device. Three zones are identified and described in the text; (b) STEM-HAADF cross section (Zone 1) corresponding to a formed device; (c) higher magnification STEM-HAADF cross section evidencing the non-coherent nature of LSMCO nanograins at Zone 1 after forming. Atomic planes are indicated with green lines and the grain boundary is marked with white dotted line; (d) sketch of the forming, RESET, and SET processes in the NSTO/LSMCO/Pt devices. After forming, epitaxial LSMCO is re-crystallized and nanograins are formed. The transition between R_{LOW} (C_{HIGH}) and R_{HIGH} (C_{LOW}) is related to LSMCO oxidation and reduction.

shows atomic images and Fast Fourier Transforms corresponding to two nanograins at Zone 1. The nanograin displayed in Figs. 4(a) and 4(b), located close to the LSMCO/NSTO interface, remains structurally very similar to pristine (oxidized) LSMCO, while the one displayed in Figs. 4(c) and 4(d), located close to the Pt top electrode, is reduced and presents an ordered structure of OV that double the LSMCO unit cell along the (001) direction, resembling previous reports in brownmillerite.³⁵ These grains are likely the source of the released O_2 during forming. Zone 3 displays a similar contrast to Zone 1 and presents an epitaxial structure with the presence of extended defects, as analyzed in supplementary material Fig. S4. All remnant resistive and capacitive states are independent of the (virgin) device area (supplementary material Fig. S5), indicating that the forming process electrically decouples Zone 1 from the rest of the device. Thus, the multi-mem behavior is confined to Zone 1, presenting an effective area of $\sim 80 \mu\text{m}^2$.

We propose that the LSMCO multi-mem behavior is related to its topotactic redox ability where oxidation (reduction) of LSMCO nanograins in Zone 1 is associated with the SET (RESET) process. This scenario is supported by memresistance experiments performed in vacuum ($< 1 \times 10^{-2}$ mbar) where it is found that the SET event is not achieved (supplementary material Fig. S6), indicating that environmental O_2 is critical for the SET process through LSMCO oxidation. Further evidence about the link between memresistance and LSMCO redox was obtained by simulating the experimental HSL [Fig. 1(b)] with the voltage enhance OV drift model,^{8,9,13} adapted to the present system. The simulation assumes a 1D chain of LSMCO nanodomains, able to accommodate different oxygen content which controls their resistivity, in contact with an oxygen reservoir (see the supplementary material for further details). The model simulates the oxygen dynamics related to the electrically induced LSMCO oxidation

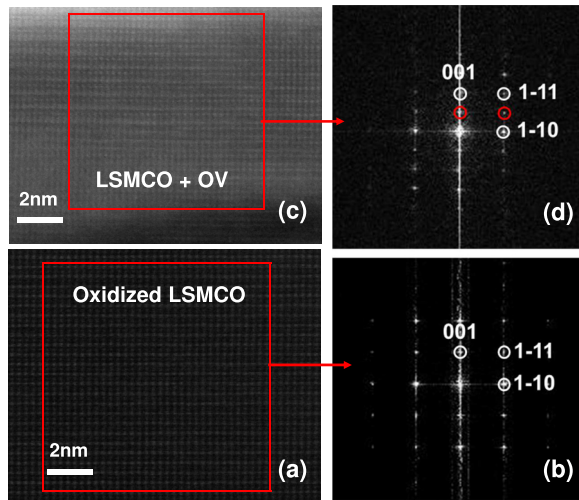


FIG. 4. (a) and (b) Atomic image and FFT, respectively, corresponding to a post-forming LSMCO nanograin (Zone 1) in contact with the NSTO substrate. An oxidized LSMCO perovskite structure is observed; (c) and (d) Same analysis for a LSMCO nanograin in contact with the Pt top electrode. The grain structure is perovskite-type, but with ordered OV that double the unit cell along the (001) direction (see additional diffraction spots, circled in red), indicating the presence of reduced LSMCO. The zone axis is $[-1,10]$ for both FFTs. These images correspond to a different lamella from that in images displayed in Fig. 3.

and reduction. The simulated HSL shows a very good agreement with the experimental one, as shown in Fig. 1(b).

Further insight into the memristive mechanism was obtained from the analysis of the I–V curves corresponding to the two resistive states, by plotting the power exponent $\gamma = d(\ln(I))/d(\ln(V))$ vs $V^{1/2}$.³⁶ This method is useful for identifying the presence of multiple conduction mechanisms,^{37–39} which often occurs at metal/complex oxide interfaces.^{40–42} Figure 5(a) shows the complex evolution of γ vs $V^{1/2}$ for both R_{HIGH} (C_{LOW}) and R_{LOW} (C_{HIGH}), indicating the presence of several circuit elements with relative weights that change between these states. The equivalent circuit that describes the γ vs $V^{1/2}$ behavior is shown in Fig. 4(e) and includes the series combination of: (i) an n-p diode in parallel with a leakage channel R_1 , corresponding to the NSTO/LSMCO interface, (ii) the series resistor R_2 associated with the Ohmic conduction of non-interfacial LSMCO plus the LSMCO/Pt interface, and (iii) a Schottky diode linked to the external Ag/NSTO contact. The experimental I–V curves were fitted by numerically solving the implicit I–V equations of the circuit (see the supplementary material), and all circuit parameters were extracted and are listed in supplementary material Table S1. Figures 5(a) and 5(b) show the excellent fits of the experimental and γ vs $V^{1/2}$ and I–V curves for both R_{HIGH} (C_{LOW}) and R_{LOW} (C_{HIGH}) states. The fittings indicate that the transition between R_{HIGH} (C_{LOW}) and R_{LOW} (C_{HIGH}) is dominated by the metallization of the LSMCO/NSTO interface, reflected in the increase in the p-n diode inverse saturation I_{satpn} from 2.5 to 5.6 μA and the decrease in the leakage resistance R_1 from 270 to 110 Ω . Impedance spectroscopy (IS) was performed to further investigate the AC response of the different multi-mem states. Figures 5(c) and 5(d) display the Cole–Cole plots for R_{HIGH} (C_{LOW}) and R_{LOW} (C_{HIGH}), respectively. The equivalent circuit that allows a good fit of the R_{LOW}

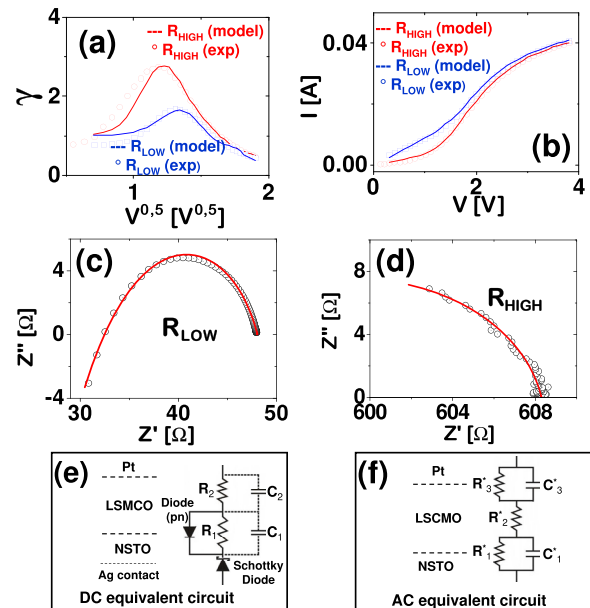


FIG. 5. (a) γ vs $V^{1/2}$ representation and (b) corresponding I–V curves for both the experimental (open symbols) and the calculated (solid line) R_{HIGH} (C_{LOW}) and R_{LOW} (C_{HIGH}) states. The fits are performed by considering the (DC) equivalent circuit presented in (e). C_1 and C_2 were included for completeness but have no effect in the low frequency range used for the I–V experiments; (c) and (d) impedance spectroscopy spectra recorded for R_{HIGH} (C_{LOW}) and R_{LOW} (C_{HIGH}) states. The experimental points are shown with open symbols, while the fittings are shown with solid lines; (f) equivalent (AC) circuit proposed to model the experimental impedance spectra. R_3^*/C_3^* corresponds to the LSMCO/Pt interface, R_1^*/C_1^* to the NSTO/LSMCO interface, and the series resistance R_2^* includes the non-interfacial LSMCO plus the contribution of the Ag/NSTO interface. We note that R_2 in (e) includes both R_2^* and R_3^* of the AC equivalent circuit of (f) and that the n-p diode AC contribution is included in R_1^* .

(C_{HIGH}) state is shown in Fig. 5(f), and was also used to simulate the R_{HIGH} (C_{LOW}) spectrum. The fitted values for the circuit elements are shown in supplementary material Table S2. Again, it is found that the multi-mem effect is mainly localized at the NSTO/LSMCO interface, characterized by the parallel combination of R_1^* and C_1^* [see Fig. 5(f)]. R_1^* changes from $\sim 10 \Omega$ to $\sim 500 \Omega$ and C_1^* from $\sim 3 \times 10^{-8} \text{ F}$ to $\sim 1 \times 10^{-12} \text{ F}$ between R_{LOW} (C_{HIGH}) and R_{HIGH} (C_{LOW}), reinforcing the idea of the presence of a switchable diode formed at the NSTO/LSMCO interface.

Thus, an oxidized NSTO/LSMCO interface leads to a R_{LOW} (C_{HIGH}) state, and a reduced interface results in a R_{HIGH} (C_{LOW}) state. The key factor for this behavior is the topotactic redox ability of LSMCO, which tolerates large changes in its oxygen content between oxidized and reduced phases. The physical origin of the large memcapacitance is intriguing and can be attributed to different effects. A possible one is related to large variations in the donor/acceptor balance at the NSTO/LSMCO interface upon LSMCO redox. The p-character of oxidized LSMCO is determined by the 0.5 holes/f.u. introduced in the lattice when Sr^{2+} ions replace La^{3+} . In the reduced phase, each OV leaves two electrons behind, and part of these electrons will recombine with existing holes, reducing the number of uncompensated LSMCO acceptors. This could strongly change the (NSTO) donor/(LSMCO)

acceptor balance at the interface, affecting the diode depletion layer and its capacitance. Other possible origin for the large memcapacitance is the Maxwell-Wagner effect, related to the creation of metallic zones embedded in the dielectric oxide, acting as the parallel plates of nanocapacitors,⁴³ that could produce large effective dielectric constants.⁴⁴ The metallization of the NSTO/LSMCO interface in the R_{LOW} (C_{HIGH}) state could take place inhomogeneously, generating an interfacial capacitance significantly larger than that expected for a homogeneous interface. Further studies are necessary to confirm and get deeper insight into these mechanisms, together with the development of strategies to circumvent the electroforming process.

See the [supplementary material](#) for additional structural and electrical characterization of our devices, together with details about the simulation and fittings of the electrical response.

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